REMARKS

This paper is responsive to the Office Action dated October 22, 2003, having a shortened statutory period expiring on January 22, 2004, wherein:

Claims 1, 3-12, 14, 15, 17-20, 22-25, and 27-29 were pending in the application.

Claims 1, 3-12, 14, 15, 17-20, 22-25, and 27-29 were rejected.

Applicants' claims 6 and 15 have been amended and no claims have been added or canceled by this amendment. Consequently, claims 27-30, 32-36, 38-43, 45-49, and 51-59 remain currently pending in the present application.

Rejection of Claims under 35 U.S.C. §102

In the present Office Action, claims 1, 3, 4, 6, 7, 9-12, and 14 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 5,951,651, issued to Lakshman et al. (hereinafter *"Lakshman"*). While not conceding that the Examiner's cited reference(s) qualify as prior art, but instead to expedite prosecution, Applicants have elected to respectfully disagree and traverse the rejection as follows. Applicants reserve the right, for example, in a continuing application, to establish that one or more of the Examiner's cited references do not qualify as prior art as to an invention embodiment previously, currently, or subsequently claimed.

Applicants respectfully submit with regard to Applicants' claim 1 that the Examiner's cited portions of *Lakshman* fail to teach the claimed method of packet processing comprising,

> parsing a packet using a first peripheral processor, said packet having a header portion, to determine a vector;
> coordinating processing using said vector;
> deconstructing said packet header to form header data using a second peripheral processor;
> searching one or more data structures based on said header data to produce search results using a third peripheral processor...
> wherein said coordinating comprises,
>> storing data within a shared register set coupled to each of said peripheral processors...and
>> monitoring said deconstructing, said searching, and said editing.

With regard to Applicants' claim 1, and the described "parsing", the Examiner states in the present Office Action that *Lakshman* teaches, "parsing a packet (col. 2, lines 21-26) using a first peripheral processor (Fig. 8a, #225), said packet having a header portion (Fig. 1; col. 1, lines 15-17), to determine a vector (col. 2, lines 25-50)." Applicants respectfully disagree. Element 225 within Figure 8a of *Lakshman* is a "pipeline register", described as being used for temporary storage of an incoming packet. Accordingly, Applicants submit that the Examiner's referenced portion of *Lakshman* not only fails to teach "a first peripheral processor" used for "parsing a packet" as claimed but fails to teach a processor of any kind.

With regard to Applicants' claim 1, and the described "deconstructing", the Examiner states in the present Office Action that *Lakshman* teaches, "deconstructing said packet header to form header data (Fig. 4, 6; col. 6, lines 35-45) using a second peripheral processor (Fig. 8b, #260 and #276)." Applicants respectfully disagree. Figure 4 of *Lakshman* is a diagram illustrating an array of windows partitioned in accordance with filter addresses. "Windows" as taught by *Lakshman* are ranges of values of a packet parameter to which one or more specific filters are applicable. (see *Lakshman*, Column 4, Lines 4-17) Figure 6 of *Lakshman* illustrates an example memory organization for the filter architecture including an array of windows to be searched, filter actions, filter specifications, and bitmap vectors for each dimension of a packet. Figure 6 of *Lakshman* is further described in the Examiner's cited portion (*Lakshman*, column 6, lines 35-45) which states,

> An example memory organization for the system is illustrated in FIG. 6, which depicts a plurality of tables 90a-90d corresponding to four dimensions associated with the following respective filter parameters: 1) source address, 2) destination addresses, 3) physical interface and source port, and, 4) protocol and destination port. Each table is shown to include an array 60a-60d of windows w_i to be searched as described above with reference to FIG. 4, the filter actions 61a-61d, the filter specifications 62a-62d and finally, the bitmap vectors 75a-75d for each dimension. The memory organization into these tables 90a-90d facilitate performing the binary search and logical AND operations in parallel.

While the referenced portions of *Lakshman* teach packet parameters or dimensions, there is no teaching of "deconstructing" a packet header as required by Applicants' claim 1. Applicants respectfully submit that the mere teaching of packet

parameters or dimensions does not teach how such parameters are generated or obtained and therefore does not teach "deconstructing" as claimed.

Applicants further respectfully disagree with the Examiner's indication that elements 260 and 276 of Figure 8b of *Lakshman* teach "a second peripheral processor" used to perform the described deconstructing. With regard to the described elements *Lakshman* teaches the following:

> Specifically, as shown in FIG. 8(b), a processing element, e.g., element 250a receives the incoming packet and stores the parameter, e.g., for dimension k=1 (source address), in a register 276. Under the control of operation controller 260 and memory control device 265, and associated memory, e.g., 90a, the binary searching method is performed whereby parameter information from the window array is input to the register 279 and comparator 280 performs a comparison to ascertain the correct window partition w_i to apply to the received packet. (emphasis supplied)

Applicants submit that the above-quoted portion of *Lakshman* clearly shows that elements 260 and 276 (an "operation controller" and a "register", respectively), are used, at most, to store a parameter and control the performance of a binary searching method to ascertain a window partition. Consequently, Applicants submit that the elements of *Lakshman* indicated by the Examiner as teaching "a second peripheral processor" (operation controller 260 and register 276) fail to teach, "deconstructing said packet header to form header data" as required by Applicants' claim.

With regard to Applicants' claim 1, and the described "editing", the Examiner states in the present Office Action that *Lakshman* teaches, "Editing said packet (where editing can be modifying the header and/or filtering packets and/or other packet modification rules) based on said search results, said header data, and said vector (col. 6, lines 29-34) using a fourth peripheral processor (Fig. 8a, #295 and #225)." Applicants respectfully disagree. More specifically, Applicants disagree with the Examiner's indication that elements 295 and 225 of Figure 8a of *Lakshman* teach "a fourth peripheral processor" used to perform the described editing.

With regard to the described elements (in addition to that which has been previously described herein regarding pipeline register 225) *Lakshman* teaches that,

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Referring back to FIG. 8(a), once the corresponding bitmap vectors are determined from each processing element 250a, . . . , 250n, for each dimension, the vectors are input to <u>logic circuitry 295 for performing the intersection, i.e., logical AND operation.</u> From the resultant bitmap vector, the CPU will apply the rule of highest priority, and performs the action dictated by the rule upon <u>the received packet stored in the pipeline register 225.</u>" (*Lakshman*, Column 6, Lines 24-31, emphasis supplied)

Applicants submit that the above-quoted portion of *Lakshman* clearly shows that elements 295 and 225 ("logic circuitry" and a "pipeline register", respectively) are used, at most, to store a received packet and to perform a logical AND operation on bitmap vectors applicable to each parameter of the received packet. Applicants submit therefore that elements 295 and 225 are used in conjunction with <u>bitmap vectors</u> rather than packets to perform a logical AND operation which fails to teach "editing" a bitmap vector, much less a packet as required by Applicants' claim. Consequently, Applicants submit that *Lakshman* fails to teach "editing said packet" as claimed.

With regard to Applicants' claim 1, and the described "coordinating", the Examiner states in the present Office Action that *Lakshman* teaches, "Coordinating processing using said vector (col. 6, lines 5-10)...Wherein said coordinating comprises: i. Storing said data within a shared register set coupled to each of said peripheral processors (Fig. 8b, #279)...and iii. Monitoring said deconstructing, said searching, and said editing (Fig. 8a, #210; Fig. 8b, #260 and #265). Applicants respectfully disagree. Column 6, Lines 5-10 of *Lakshman* teaches that,

FIG. 8(a) illustrates the hardware device 200 for implementation in a packet forwarding engine or router, including an input line 205 for receiving an incoming packet and a bi-directional CPU interface line 210 representing control and timing lines for purposes of illustration. The incoming packet is input to a pipeline register 225 for temporary storage and is also input to each processing element indicated as elements 250a, . . . , 250n corresponding to each dimension k=1 to k=n.

While *Lakshman* elsewhere describes "bitmap vectors" (see, e.g., *Lakshman*, Column 2, Lines 33-38) Applicants respectfully submit that the above-quoted portion of *Lakshman* as well as the descriptions of the other elements referenced by the Examiner (bi-directional CPU interface line 210 of Figure 8a and register 279, operation controller

260, and memory control device 265 of Figure 8b of *Lakshman*) fail to teach the use of such bitmap vectors, or any other vectors, in coordinating processing where such "coordinating" includes *inter alia* "monitoring said deconstructing, said searching, and said editing" as required by Applicants' claim.

Accordingly, Applicants submit that claim 1 is allowable over *Lakshman* and that Applicants' claim 6, including one or more elements or limitations substantially similar to those previously described herein, is similarly allowable. Applicants further submit that all remaining claims, depending directly or indirectly from Applicants' claims 1 or 6 are allowable for at least the reasons stated for the allowability of the corresponding claim(s) from which they depend.

Rejection of Claims under 35 U.S.C. §103

In the present Office Action, Applicants' claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over *Lakshman* in view of U.S. Patent No. 6,226,267, issued to Spinney et al. (hereinafter "*Spinney*") and Applicants' claim 8 was rejected under 35 U.S.C. 103(a) as being unpatentable over *Lakshman* in view of U.S. Patent No. 6,421,730, issued to Narad et al. (hereinafter "*Narad*"). While not conceding that the Examiner's cited reference(s) qualify as prior art, but instead to expedite prosecution, Applicants have elected to respectfully disagree and traverse the rejection as follows. Applicants reserve the right, for example, in a continuing application, to establish that one or more of the Examiner's cited references do not qualify as prior art as to an invention embodiment previously, currently, or subsequently claimed.

With regard to Applicants' claim 5, the Examiner states in the present Office Action that,

> Spinney teaches that said coordinating further comprises operating on said search argument to form a modified search argument prior to said searching, and said searching uses said modified search argument (col. 2, lines 20-35). Lakshman does not go into enough detail regarding the search technique to adequately disclose this item. At the time the invention was made, one of ordinary skill in the art would have used the Spinney search process to learn how to implement the Lakshman search process, and to allow the type of flow to be a searching parameter (col. 2, lines 49-65).

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Applicants respectfully disagree. As an initial matter, Applicants note that the Examiner has failed to indicate if, and if so where, any of the Examiner's cited references teach, show, or suggest a method of packet processing comprising "forming a search argument" as required by Applicants' claim 5. Moreover, in the present Office Action the Examiner has failed to provide any suggestion or motivation whatsoever for the proposed combination of the teachings of *Spinney* and *Lakshman* as required by a *prima facie* case of obviousness under 35 U.S.C. §103.

Applicants further submit that the Examiner's cited portions of *Spinney* (*Spinney*, Column 2, Lines 20-35 and 49-65) fail to teach, show, or suggest, "operating on said search argument to form modified search argument prior to said searching" as claimed. Spinney *teaches* in the Examiner's cited portions rather only that, "the invention classifies received frames into flows based not only on the Layer 2 MAC or Layer 3 network address, but also on the information contained in higher layers, even up to 'Application' Layer 7 of the OSI model" and "comparing hashed versions of the canonical headers to identify the packets to flows with common flow rules." Applicants respectfully request that the Examiner cite with specificity where and how the Examiner's cited references teach, show, or suggest "forming" and/or "operating" as claimed.
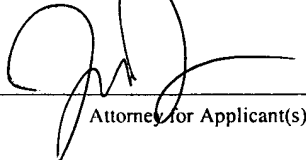
Accordingly, Applicants submit that claim 5 is allowable over *Lakshman* and that Applicants' claim 19 and 24, each including one or more elements or limitations substantially similar to those previously described herein, are similarly allowable for at least the reasons stated for the allowability of claim 5.

In the present Office Action, the Examiner further states that, "As to claims 15, 17-20, 22-25, 27-29, they do not teach or define above the correspondingly rejected claims 1 and 3-5 and thus claims 15, 17-20, 22-25, 27-29 are rejected for the reasons above." Applicants submit that it is unclear how the Examiner intended to apply the above-quoted statement to Applicants' claims as it appeared within a section of the present Office Action titled, "Claim Rejections – 35 USC § 103" while referencing the Examiner's rejection of claim 1 under 35 U.S.C. § 102. To the extent the Examiner intended, by the above-quoted statement, to reject Applicants' independent claims 15, 20
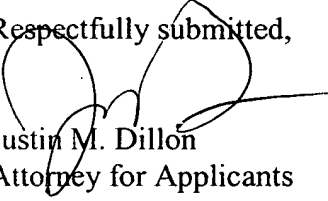
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and/or 25 under 35 U.S.C. §102 or §103 as described above however, Applicants submit that the described claims are allowable for at least those reasons previously set forth herein.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5080.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Non-Fee Amendment, COMMISSIONER FOR PATENTS, P. O. Box 1450, Alexandria, VA 22313-1450, on January 22, 2004.

Attorney for Applicant(s)   Date of Signature
1-27-04

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